REMARKS/ARGUMENTS

Amendments

The claims are modified in the amendment. More specifically, claims 4, 5, 7 and 8 have been amended to address the claim objections in the final Office Action, among other things. These corrections, being merely grammatical in nature, are not believed to affect claim scope. Therefore, claims 1-19 are present for examination. No new matter is added by these amendments and clarifies the issues for appeal. Applicant respectfully requests entry of the amendments and reconsideration of this application as amended.

35 U.S.C. §103 Rejections, Baltz et al., Kozyrakis et al., Hsu et al., & Hagersten et al.

The final Office Action has rejected claim 1 under 35 U.S.C. §103(a) as being unpatentable over the cited portions of U.S. Patent No. 6,321,318 to Baltz et al. (hereinafter "Baltz") in view of the cited portions of non-patent literature document entitled "Scalable Processors in the Billion-Transistor Era: IRAM" to Kozyrakis (hereinafter "Kozyrakis"). Further, the final Office Action has rejected claims 2-15 under 35 U.S.C. §103(a) as being unpatentable over the cited portions of U.S. Patent No. 5,710,907 to Hagersten et al. (hereinafter "Hagersten") in view of the cited portions of U.S. Patent No. 6,128,700 to Hsu et al. (hereinafter "Hsu") and further in view of Kozyrakis. Further still, the final Office Action has rejected claims 16-19 under 35 U.S.C. §103(a) as being unpatentable over Hagersten in view of Kozyrakis.

The patent office is charged with putting forth a *prima facie* showing of obviousness. Applicants believe a *prima facie* case of obviousness has not been properly set forth in the final Office Action. The basic test is excerpted below:

> "To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations." See MPEP §2143, Original Eighth Edition, August, 2001, Latest Revision February 2003.

Applicants believe the rejection has flaws with at least two of the three prongs of the above test for establishing a *prima facie* case of obviousness. More specifically, Kozyrakis teaches away from any combination, and Kozyrakis asserts that there would not be any reasonable expectation of success in any such combination.

Motivation to Combine Kozyrakis with Other References

The first prong of the test requires, a suggestion or motivation to combine references to avoid hindsight reconstruction of the claimed invention based upon the information disclosed in the present application. Any motivation found in Kozyrakis must be tempered by teaching away in that same reference. Many instances of teaching away were found that would make it unreasonable to presume that one of ordinary skill in the art would arrive at the combination suggested in the final Office Action.

Kozyrakis emphasizes that the *entire* memory on the chip has advantage over those that cache on-chip with an external memory. Kozyrakis, page 75, right column, last full paragraph, last sentence. Kozyrakis goes on to further denigrate on-chip caching by indicating that increasing the size of on-chip cache doesn't solve the problems with this configuration. Kozyrakis, page 76, left column, first full paragraph. The claimed invention requires the ability to switch to between on-chip memory and on-chip cache with external memory. It is not reasonable to combine a teaching from Kozyrakis with references that teach on-chip caching with external memory given this express teaching away.

In further distinguishing on-chip caching with external memory, Kozyrakis emphasizes that on-chip memory has low latency, reduces energy consumption, and has simpler interfaces and pin count. Kozyrakis, page 76, left column, first paragraph. These three additional instances of teaching away make it even less likely that one of ordinary skill would make the suggested combination. Applicant respectfully posits that use of Kozyrakis in combination with references that perform on-chip caching does not provide motivation for a combination given this extensive teaching away.

Reasonable Likelihood of Success in Combining Kozyrakis with Other References

The second prong of the test requires a reasonable likelihood of success in performing any combination without undue experimentation. Kozyrakis is apparently a theoretical article that never actually achieves integrated memory in any mainstream way. Kozyrakis emphasizes "critical issues" required to have any likelihood of success with this approach. Kozyrakis, page 77, left column, last full paragraph, through right column, last full paragraph. Specifically, performance issues of DRAM transistors, noise reduction, yield reduction, bounded DRAM issues, etc. are all listed as "critical issues." Given all these "critical issues" what reasonable chance would anyone have with using the teachings of Kozyrakis in achieving the claimed invention without undue experimentation.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is urged. Reconsideration of the claims in their current form is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 303-571-4000.

Respectfully submitted,

Thomas D. Franklin
Reg. No. 43,616

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: 303-571-4000
Fax: 415-576-0300
TDF:cmb
60219849 v1